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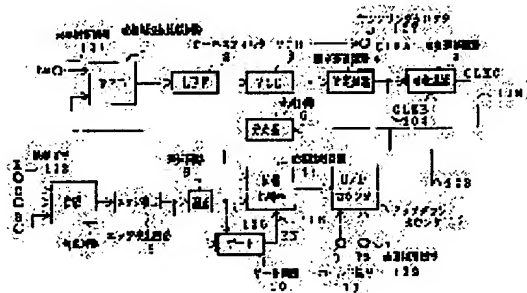|	
(21)Application number : **07-215087**	(71)Applicant : **SEIKO EPSON CORP**
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(54) DOT CLOCK REPRODUCING CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To reproduce a dot clock which can perform sampling in a noise nonproducing phase even when ringing or the like by characteristics of an output circuit of a device and a connecting cable is caused in the case of obtaining a sampling clock to display a picture signal of a personal computer and a work station.

SOLUTION: A fixed delay circuit 4 and a variable delay circuit 5 are arranged in a loop of a PLL circuit composed of a phase frequency comparing circuit 1, a low-pass filter 2, a VCO 3 and a dividing circuit 6. On the other hand, the edge is detected from a picture signal 102 by an edge detecting circuit 8, and a phase with a CLKB 104 is compared with it by a phase comparing circuit 11, and delay time of the variable delay circuit 5 is controlled so that phases coincide with each other. A sampling clock 107 becomes a phase always advancing by fixed time more than the edge of the picture signal when it is obtained from the input side of the fixed delay circuit 4, and sampling can be performed in a position uninfluenced by ringing.